BLIP TESTING PROCEDU IBAPACAP: BOARD #		8 Oct. 19 DATE	
C INNER:			
<ul> <li>the Breakout Box (100mV/div)</li> <li>Triggers will be used that a Insure that a working Monitor 0</li> <li>CI/CO Range note: Low =</li> <li>IMPLANT Range note: Los small that IMPLANT MON wild divider circuit. U90 is located board.</li> <li>Triggers are generated by F</li> </ul>	ON on the front panel (5V/div.) using an oscilloscope (100uS/d re generated by write commands Card is installed in the crate.  499/90.499k, High = 499/18.2 ow = 1/43.2k, High = 1/7.15k. Il be measured at pins 7 & 11 of on the bottom side, middle section PUSHING the Trigger button on a Monitor Card, or run the LED	iv). s to the Monitor 99k The output puls U90 which is p on of the top po	ce is so rior to the ortion of the ard, or by
2. Power up settings:		CIDAC CI RANGE CI PULSE Delay Trig	10V 0(low) 0(disabled) 0(disabled)
3. Test preparation settings:		<u>, , , , , , , , , , , , , , , , , , , </u>	/
Set to high range: Turn pulse enable on:	CinnerDAC(10) ciRange(1) ciPulse(1) trigDelay(0)	CIDAC CI RANGE CI PULSE Delay Trig	10V 1(high) 1(enabled) 0(disabled)
Turn Delay Trigger on.	nigDemy(v)		
4. C INNER test: Input settings in Step 3 before sta	arting test.	CIDAC CI RANGE	10V 1(high)
Sand triaggraphs IDADACAD	mass the manual button on the	CLPHESE	1(enabled)

Delay Trig 0(disabled)

Send triggers to IBAPACAP: press the manual button on the monitor card

or

module X

LEDpulse(20)

Note: X is the slot that the monitor card is in, to make changes to the blip card change the module setting back to the slot number that the card is in.

BLIP TESTING PROCEDURE IBAPACAP: BOARD #	CDMS STATUS	8 Oct. DATE _		
Record output waveform:  Expected output is a ramped squarewave with a flattop 400us, with an amplitude of:CIMON=10V, AUX.=300mV.	V	ON(fp)	AUX.(bb)	
5. Range test:		CIDAC	10V	
Input settings in Step 3 before starting	test.	CI RANG	` /	
-	e X ulse(20)	CI PULSI Delay Trig	` /	
Note: X is the slot that the monitor card is in.  Does the amplitude of either output change?				
Which one and what is new am	mplitude?			
6. DAC test:		CIDAC	1-5V	
Input settings in Step 3 before starting	test.	CI RANG		
		CI PULSI	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	
Set DAC to various settings from 0 to 10 measurements from the front panel an	d from the breakout	Delay Trig	` /	
1 (DOD)	aDAC(v)			
box(BOB): Cinner	DAC(x)	DAC   Ci	Mon BOB	
· ,	. ,	DAC Ci	Mon BOB	
Send triggers to IBAPACAP: module	e X	0 2	Mon BOB	
Send triggers to IBAPACAP: module LEDpu	e X ulse(20)	0 2 5	Mon BOB	
Send triggers to IBAPACAP: module	e X ulse(20)	0 2 5 7	Mon BOB	
Send triggers to IBAPACAP: module <i>LEDpu</i>	e X ulse(20)	0 2 5	Mon BOB	
Send triggers to IBAPACAP: module LEDpt  Note: X is the slot that t	e X ulse(20)	0 2 5 7 10		
Send triggers to IBAPACAP: module <i>LEDpu</i>	e X ulse(20) the monitor card is in.	0 2 5 7	10V	

Note: Adjustment of R43 will delay the pulse from 363 mSeconds Delay Trig to 36.7 Seconds.

Adjust R43 so the voltage measured at junction of R44 and R43 is 5V.

Turn Delay Trigger on:	trigDelay
Turn Delay Trigger on:	irigDetay

CI PULSE 1(enabled) 1(enabled)

IBAPACAP: BOARD # _			8 Oct. 199 DATE	
<b>Send a trigger</b> by using the trig how long the before the puls	_		Observe the outpo	ut and time
Adjust R43 so the voltage measu	ared at junction of R	44 and R43 i	s 0.05V.	
<b>Send a trigger</b> by using the trig how long the before the puls	_		Observe the outpo	ut and time
C OUTER:				
<ul> <li>Test connections and set up:</li> <li>Measure COUTER at Con the Breakout Box (100m)</li> <li>Triggers will be used that Insure that a working Monito</li> <li>CI/CO Range note: Low</li> <li>Triggers are generated be sending write commands to way).</li> </ul>	COMON on the front V/div) using an oscilute are generated by wor Card is installed in a 499/90.499k, Hisy PUSHING the Trigon.	lloscope (100 rite command the crate. gh = 499/18. gger button o	uS/div). ds to the Monitor 299k n the Monitor Ca	Card. rd, by
2. Power up settings:			CODAC CO RANGE CO PULSE Delay Trig	10V 0(low) 0(disabled) 0(disabled)
3. Test preparation settings:				
readfile ibapacap.macro Set CO DAC to 10V: Set to high range: Turn pulse enable on: Turn Delay Trigger off:	CouterDAC(10) coRange(1) coPulse(1) trigDelay(0)		CODAC CO RANGE CO PULSE Delay Trig	10V 1(high) 1(enabled) 0(disabled)
4. C OUTER test:				
Input settings in Step 3 before	starting test.		CODAC CO RANGE	10V 1(high)
Send triggers to IBAPACAP:	press the manual monitor card	button on the	CO DITI CE	1(enabled) 0(disabled)
or	module X			
Note:	LEDpulse(20) X is the slot that the	monitor car	d is in	
Note.	A is the stot that the	e monnor car	a is iii.	

	CDMS ATUS		ct. 1998	
Record output waveform:	COI	MON(fp)	AUX.(bb)	
Expected output is a ramped squarewave with a flattop of 400us, with an amplitude of: COMON=10V, AUX.=300mV.		t	t	
5. Range test:				
Input settings in Step 3 before starting test.		CODA CO RA		ow)
Select low Range: coRange(0)		CO PU Delay	`	nabled) abled)
Send triggers to IBAPACAP: module X  **LEDpulse(20) N	ote: X is the s			
Does the amplitude of either out: Which one and what is new amplit	-	e?	_	
6. DAC test:		CODA	.C 1-5V	
Input settings in Step 3 before starting test.		CO RA	NGE 1(hi	gh)
Set DAC to various settings from	0 to 10V	CO PU	`	nabled)
and record: CouterDAC(		Delay	Trig O(disa	abled)
Send triggers to IBAPACAP: module X		DAC	Co Mon	BOB
LEDpulse(20	))	0		
Note: X is the slot that the mon	itor card is in	. 2 5		

## **IMPLANT SECTION:**

- 1. Test connections and setup:
  - IMPLANT RANGE note: The output pulse is so small that IMPLANT MON will be measured at pins 7 & 11 of U90 which is prior to the divider circuit. U90 is located on the bottom side, middle section of the top portion of the board. The voltage dividers are: Low = 1/43.2k, High = 1/7.15k.
  - Monitor IMPLANT output at IMPLANT MON. on front panel.
- 2. Power up settings:

IMPLANTDAC OUT	10V
HEAT DC	0(off)
IMPLANT PULSE ENA	0(disabled)
IMPLANT RANGE	0(low)

7 10

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3. Test preparation settings:			
readfie implant.macro			
Set IMPLANT DAC to 5V:	ImplantDAC(5)	IMPLANTDAC OUT	5V
Turn HEAT DC off:	pHeat(0)	HEAT DC	0(off)
Enable pulse:	pPulse(1)	IMPLANT PULSE ENA	` ′
Select high range:	pRange(1)	IMPLANT RANGE	1(high)
4. DC HEAT test:	_	IMPLANTDAC OUT	5V
Input settings in Step 3 before s	starting test.	HEAT DC	1(on)
T. HEATING	TT	IMPLANT PULSE ENA	` ′
Turn HEAT DC on:	pHeat	IMPLANT RANGE	1(high)
Record the measurement the front panel and U90.	<del>-</del>	DAC Implant Mon. Pin7 11 0 1	Pin
Set IMPLANT DAC to different values from 0V to 10V and record the measurements.		3   5   7   10	
Are the measurements ed	qual in amplitude:	10	
5. Send Pulses:	4. 4 4 4	IMPLANTDAC OUT	5V
Input settings in Step 3 before s	starting test.	HEAT DC	0(off)
Disable HEAT DC: pHo	eat(0)	IMPLANT PULSE ENA	1(enabled)
Enable pulse: pPi		IMPLANT RANGE	1(high)
Send triggers to IBAPACAP: mo			
	<b>Dpulse(20)</b> Note: X is the slot i	that the monitor card is in.	
Are pulses observed at	the measuring points	?	
6. RANGE test:			
Input settings in Step 3 befo	re starting test.	IMPLANTDAC OUT 5V	
		HEAT DC 1(c	on)
Turn HEAT DC on:	pHeat	IMPLANT PULSE ENA	1(enabled)
	_	IMPLANT RANGE 1 &	2 0
Measure the outputs of U90 p  Are the outputs equa	ins 6, 7. i <b>1?</b> <u>yes</u> , condit	cion OK)	
Measure the outputs of U90 p  Are the outputs equa	ins 10, 11. i <b>1?</b> ( <u>yes</u> , conditio	on OK)	

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Select low range: $pRange(\theta)$ Measure pins 6 and 10 of U90.
Did the outputs on pins 6 & 10go away? ( $\underline{\text{yes}}$ , condition OK)
7. Continuity test:  Use a DMM to measure continuity from the junction of R233 and R236 to pin 18 of P1.  Is there continuity?
Use a DMM to measure continuity from the junction of R235 and R237 to pin 34 of P1.  Is there continuity?